AMENDMENTS

IN THE CLAIMS:

Please amend the pending claims as indicated below:

1. (Currently amended) A heterojunction bipolar transistor (HBT), comprising:

a collector formed over a substrate;

a base formed over the collector;

an emitter formed over the base; and

a tunneling suppression layer between the collector and the base, the tunneling suppression layer fabricated from a material that is different from a material of the base and that has an electron affinity equal to or greater than an electron affinity of the material of the base, in which the collector comprises indium phosphide, the base comprises gallium arsenide antimonide, the emitter comprises two or more of indium, phosphorous, aluminum, gallium, nitrogen and arsenic, and the tunneling suppression layer comprises aluminum, gallium indium arsenide having the composition $Al_{0.33}Ga_{0.15}In_{0.52}As$.

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Currently amended) ~~The HBT of claim 2,~~ A heterojunction bipolar transistor (HBT), comprising:

a collector formed over a substrate;

a base formed over the collector;

an emitter formed over the base; and

a tunneling suppression layer between the collector and the base, the tunneling suppression layer fabricated from a material that is different from a material of the base and that has an electron affinity equal to or greater than an electron affinity of the material of the base, in which the collector comprises indium phosphide, the base comprises gallium arsenide antimonide, the emitter comprises two or more of indium, phosphorous, aluminum, gallium, nitrogen and arsenic, and ~~in which~~ the tunneling suppression layer comprises aluminum indium arsenide phosphide.

9. (Original) The HBT of claim 8, in which the tunneling suppression layer comprises indium phosphide and aluminum indium arsenide having between 40% and 100% indium phosphide.

10. (Original) The HBT of claim 9, in which the tunneling suppression layer comprises indium phosphide and aluminum indium arsenide having 58% indium phosphide and 42% aluminum indium arsenide near the base and 75% indium phosphide and 25% aluminum indium arsenide near the collector.

11. (Canceled)

12. (Currently amended) The HBT of claim 27 ~~11~~, in which the digital alloy composite comprises $Al_{0.33}$ $Ga_{0.15}$ $In_{0.52}$ As, using alternating layers of $Al_{0.48}In_{0.52}As$ and $Ga_{0.47}In_{0.53}As$.

13. (Currently amended) A method of making a heterojunction bipolar transistor, the method comprising:

providing a substrate;

forming a subcollector over the substrate;

forming a collector over the subcollector;

forming a tunneling suppression layer over the collector;

forming a base over the tunneling suppression layer; and

forming an emitter over the base,

wherein the tunneling suppression layer is formed using a material that is different from a material of the base and that has an electron affinity equal to or greater than an electron affinity of the material of the base, further comprising forming the collector using indium phosphide, forming the base using gallium arsenide antimonide, forming the emitter using a material comprising two or more of indium, phosphorous, aluminum, gallium, nitrogen and arsenic, and forming the tunneling suppression layer using aluminum indium arsenide phosphide.

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Currently amended) The method of claim 13 ~~15~~, in which forming the tunneling suppression layer comprises forming the tunneling suppression layer with a graded electron affinity, χ.

19. (Canceled)

20. (Canceled)

21. (Currently amended) The method of claim 13 ~~20~~, further comprising forming the tunneling suppression layer using indium phosphide and aluminum indium arsenide having 40% to 100% indium phosphide.

22. (Original) The method of claim 21, in which the tunneling suppression

layer comprises indium phosphide and aluminum indium arsenide having 58% indium phosphide and 42% aluminum indium arsenide near the base and 75% indium phosphide and 25% aluminum indium arsenide near the collector.

23. (Currently amended) ~~The method of claim 14,~~ A method of making a heterojunction bipolar transistor, the method comprising:

providing a substrate;

forming a subcollector over the substrate;

forming a collector over the subcollector;

forming a tunneling suppression layer over the collector;

forming a base over the tunneling suppression layer;

forming an emitter over the base, wherein the tunneling suppression layer is formed using a material that is different from a material of the base and that has an electron affinity equal to or greater than an electron affinity of the material of the base; and

forming the collector using indium phosphide, forming the base using gallium arsenide antimonide, forming the emitter using a material comprising two or more of indium, phosphorous, aluminum, gallium, nitrogen and arsenic, and ~~further comprising~~ forming the tunneling suppression layer using a digital alloy composite comprising aluminum gallium indium arsenide.

24. (Original) The method of claim 23, further comprising forming the digital alloy composite using alternating layers of $Al_{0.48}In_{0.52}As$ and $Ga_{0.47}In_{0.53}$.

25. (Currently amended) A tunneling suppression layer, comprising $Al_{0.33}Ga_{0.15}In_{0.52}As$ ~~two or more of aluminum, gallium, indium, nitrogen, phosphorous, arsenic and antimony~~.

26. (Canceled)

27. (New) A heterojunction bipolar transistor (HBT), comprising:

a collector formed over a substrate;

a base formed over the collector;

an emitter formed over the base; and

a tunneling suppression layer between the collector and the base, the tunneling suppression layer fabricated from a material that is different from a material of the base and that has an electron affinity equal to or greater than an electron affinity of the material of the base, in which the collector comprises indium phosphide, the base comprises gallium arsenide antimonide, the emitter comprises two or more of indium, phosphorous, aluminum, gallium, nitrogen and arsenic, and the tunneling suppression layer is formed of a digital alloy composite comprising aluminum gallium indium arsenide.